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Design and Analysis of Low Power Latch Sense Amplifier

Kamal Pandey[1], Vishal Yadav[2]
[1](*Department of Electronics & Communication, Shambhunath Institute of Engineering & Technology Allahabad)*
[2](*PG Student Department of Electronics & Communication, Shambhunath Institute of Engineering & Technology Allahabad)*

Abstract: *Technology scaling has enabled us to integrate both memory and logic circuits on a single chip. However, the performance of embedded memory and its peripheral circuits can adversely affect the speed and power of the overall system. Sense amplifier is one of the important peripheral circuits in the memory as it strongly influences the memory access times. It retrieves the stored data from the memory array by amplifying the small differential signal on the bit lines.*
Therefore, the power dissipated within the on-chip caches, both active and standby will become dominant parts of the total power consumption of the chip. In view of the above, there apparent urgency to address the power dissipation of chip.
The main objective of this paper is the design of Low Power Sense Amplifier. For lowering the power dissipation three techniques are used voltage scaling, half Vdd precharge circuits and VTCMOS. The most efficient way of reducing power dissipation is by scaling down the power supply voltage.
Keywords: *Low Power Technology, Tanner Tools*

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I. Introduction

Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it comes to memory sense-amp design. With increased memory capacity usually the increased bit-line parasitic capacitance. This increased bit-line capacitance in turn slows down voltage sensing and makes bit-line voltage swings energy expensive resulting in slower more energy hungry memories

Sense amplifiers are mainly used to read the contents of RAM and DRAM. They are very sensitive to noise and their design implies that they will provide adequate noise margins and provide good quality of data that represent the contents of a particular memory cell. Fast sense amplifiers are important for achieving low latency in many circuits, the most common domain being bit-line reading in memories. With the advent of sub micrometer CMOS chips, interconnection is becoming a major source of on-chip delay, and fast sense amplifiers are also likely to be needed, e.g. as repeaters for high-speed signals which must traverse large chips.

Several operate in current-mode, i.e. they present a low impedance to the inputs and respond to the differential current rather than to the voltage between the inputs , this can reduce interconnect delay in long wires there by providing speed improvement. The current mode sense amplifier reduces the bit line swing during read operation as compared to voltage mode sensing technique. It proves that current sensing technique would be faster than voltage mode due to the low impedance termination of the current mode. It shows that current sensing is relatively insensitive to the bit line capacitance. This gives the motivation to use current mode sensing in the bit lines in SRAM. The speed of the sensing operation depends on the ability of the sense amplifier as to how fast it can resolve or decide as to which of the two bit lines current is higher in magnitude and accordingly provide a logic value of "1" or "0" in the output.

II. Low Power Technique

There are three techniques which are used as a low power design.

Half Precharge Voltage

If we use precharge voltage for precharge circuit half of the VDD then improvement in power dissipation but also read time increase little bit take place. Because when WL and sense amplifier is enabled then one of bit lines is going for ground and other going for high potential of VDD. So with this difference between the bit lines created so fast. With this sense amplifier latched the outputs quickly. So with this fast operation the power dissipation is also decrease. But we cannot decrease the precharge voltage below the half of

VDD because with this cell's internal data is disturbed or it may reside in metastable values. So it is urgent to check while using the concept of half precharge voltage.

Substrate Biasing (VTCMOS)

Out of various techniques to minimize the leakage and sub-threshold currents to minimize static power dissipation one can use variable threshold CMOS (VTCMOS) circuit which is easier to achieve and is discussed here.

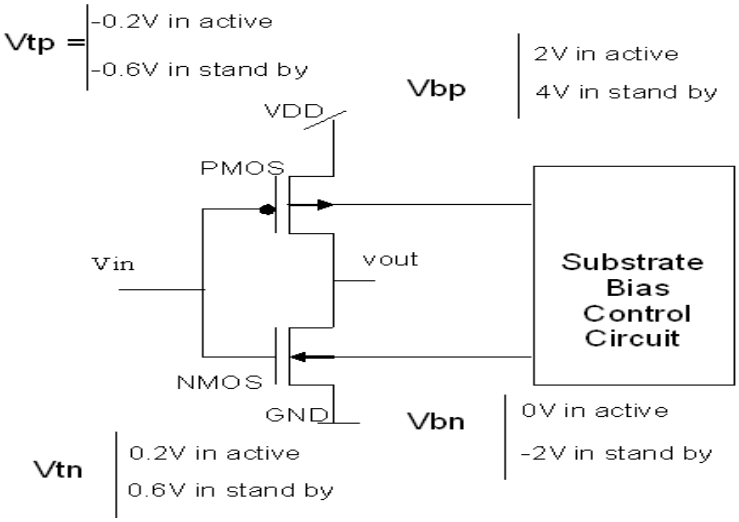

Figure 2 VT CMOS

The basic principle of VTCMOS circuit is to keep the substrate Separate from source and apply different voltage to it with respect to source. Here the substrates of PMOS and NMOS transistors are separated out and having their own voltage source called substrate bias control circuit.

Voltage Scaling

In Voltage Scaling we are primarily concerned with the contributions of capacitance to the power expression CV^2f. Clearly, though, the reduction of V should yield even greater benefits; indeed, reducing the supply voltage is the key to low-power operation, even after taking into account the modifications to the system architecture, which is required to maintain the computational throughput. First, a review of circuit behavior (delay and energy characteristics) as a function of scaling supply voltage and feature sizes.

III. Latch Sense Amplifier

The drains of transistors MP1, MN5, MP2 and MN4 are output nodes. There is no current flow from bit lines to output nodes. When sensing signal SE is at logic 0 (GND), the output node is isolated to GND, and the pre charge transistors MP3, MP4 charge output nodes to V_{DD}. Because the output nodes *out* and outb are pre charged to V_{DD}, the transistors MP1, MP2 are at cut-off region and MN4, MN5 are at saturation region. When the sensing signal SE changes to logic 1 (V_{DD}), MN3 is turned on and the node S is pulled down to GND level. Under this condition, MN1 and MN2 are working as a common source differential amplifier

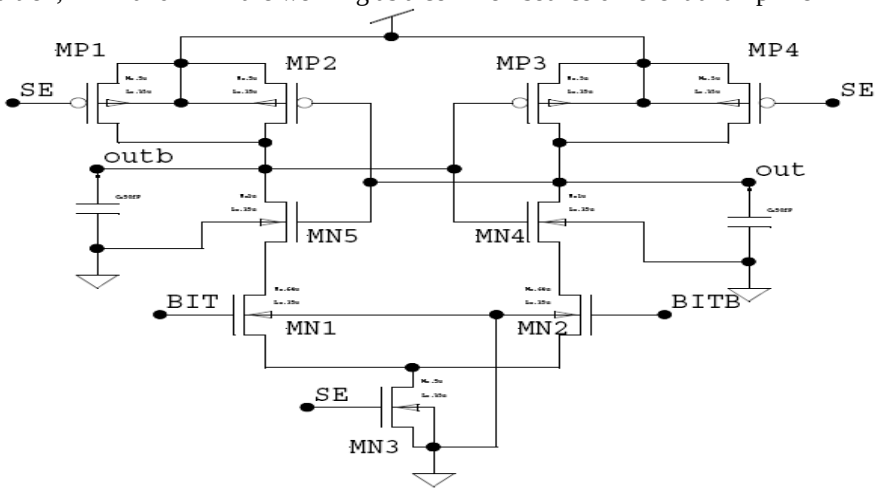

Figure3 Latch Sense Amplifier

IV. Low Power Latch Sense Amplifier

In proposed design as for as concerned about the low power dissipation we use three techniques that is voltage scaling, half V_{DD} precharged circuits and VTCMOS. For solving the problem of leakage power dissipation in standby mode we use a technique of VTCMOS. In standby mode it provides -0.9v to transistor of body terminal so with this the V_{th} of the transistor increase so the power dissipation decreases. In normal mode body terminal is connected to the ground, so nobody effects is occurred in the working of the sense amplifier. In precharge circuits we use half voltage of the V_{DD} to reduce the power dissipation in the sense amplifier.
Proposed sense amplifier is shown in figure 4.

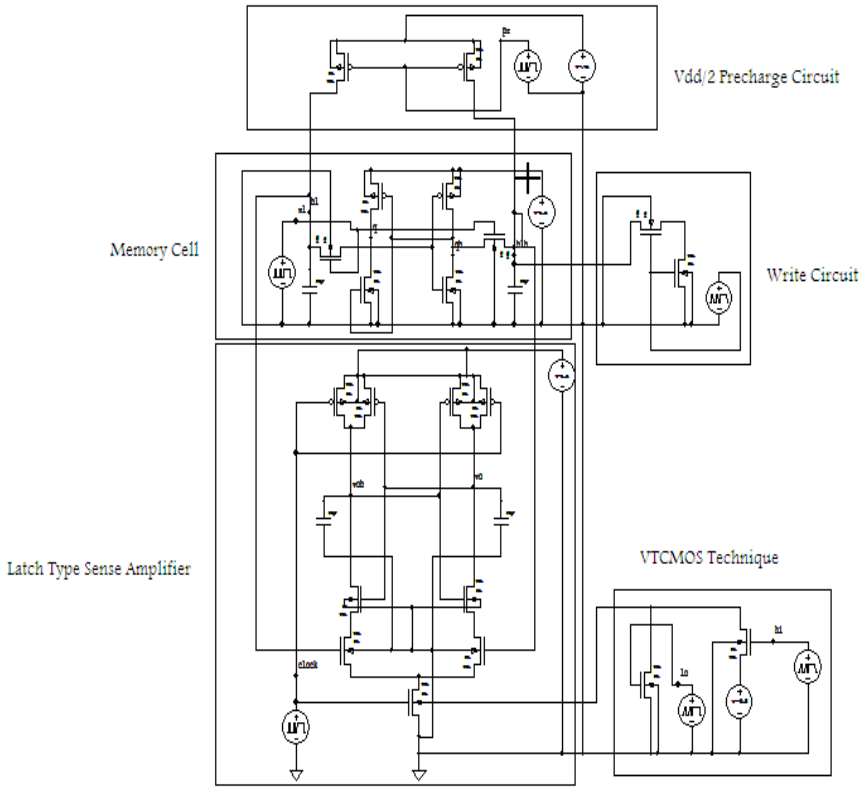

Figure4 Low Power Latch Sense Amplifier

Latch type sense amplifier has less power so it is selected as proposed design for applying low power techniques. In voltage mode sense amplifier, the circuit amplifies a small differential voltage in the bit lines to a full swing output. Current mode sense amplifier, it amplifies a small differential current in the bit lines to a minimal swing. These circuits are faster as differential currents develop faster than voltage.

V. Results and calculation

Voltage Waveform:

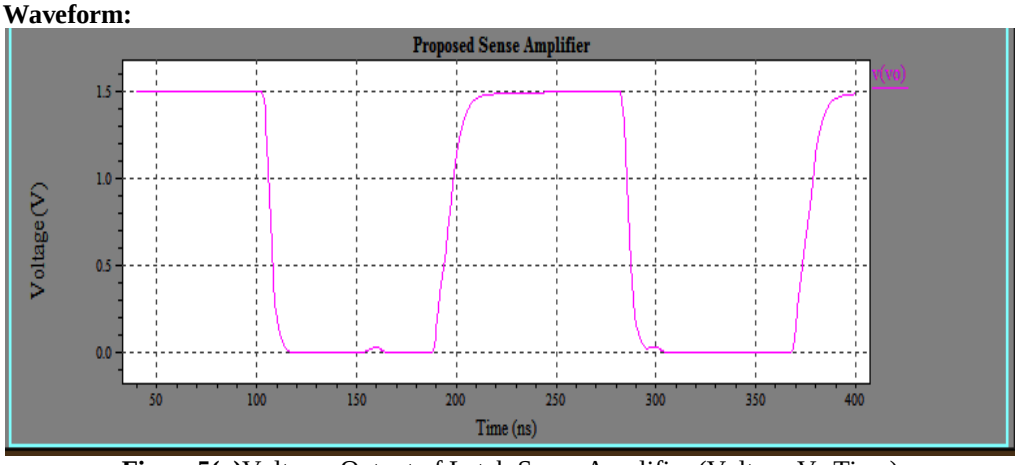

Figure5(a) Voltage Output of Latch Sense Amplifier (Voltage Vs Time)

Current Waveform:

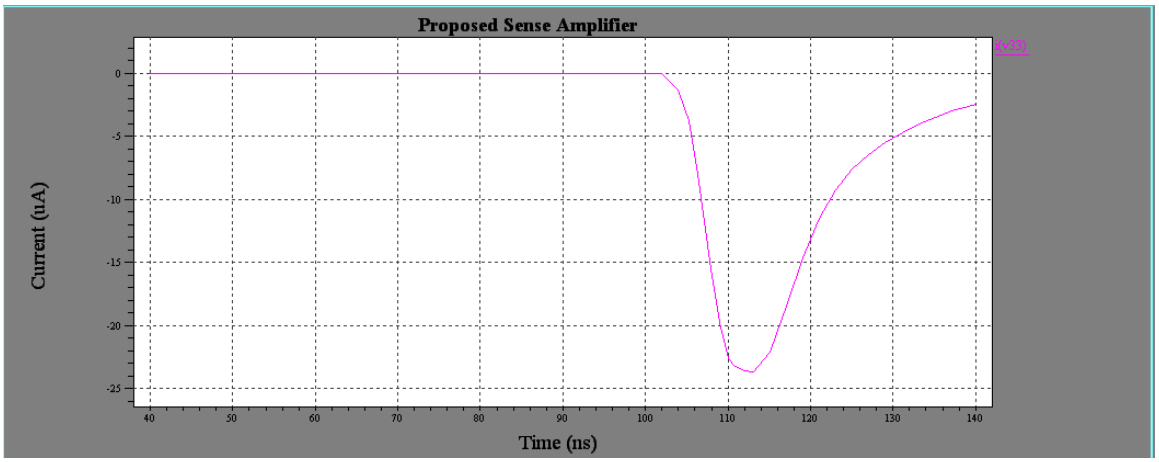

Figure5 (b) Current Output of Latch Sense Amplifier (Current Vs Time)

Power Waveform:

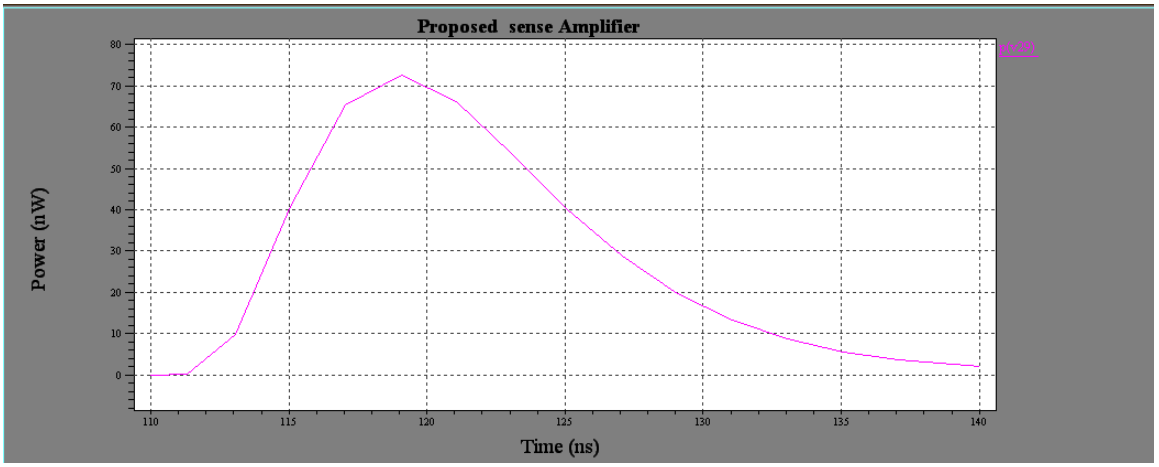

Figure5 (c) Power Output of Latch Sense Amplifier (Power Vs Time)

Calculation of Propagation Delay:

Rise time

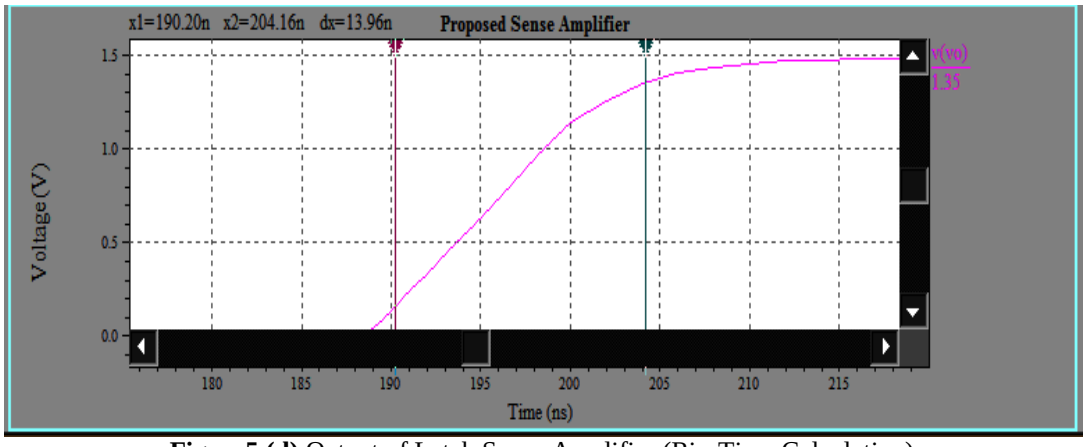

Figure5 (d) Output of Latch Sense Amplifier (RiseTime Calculation)

Fall Time

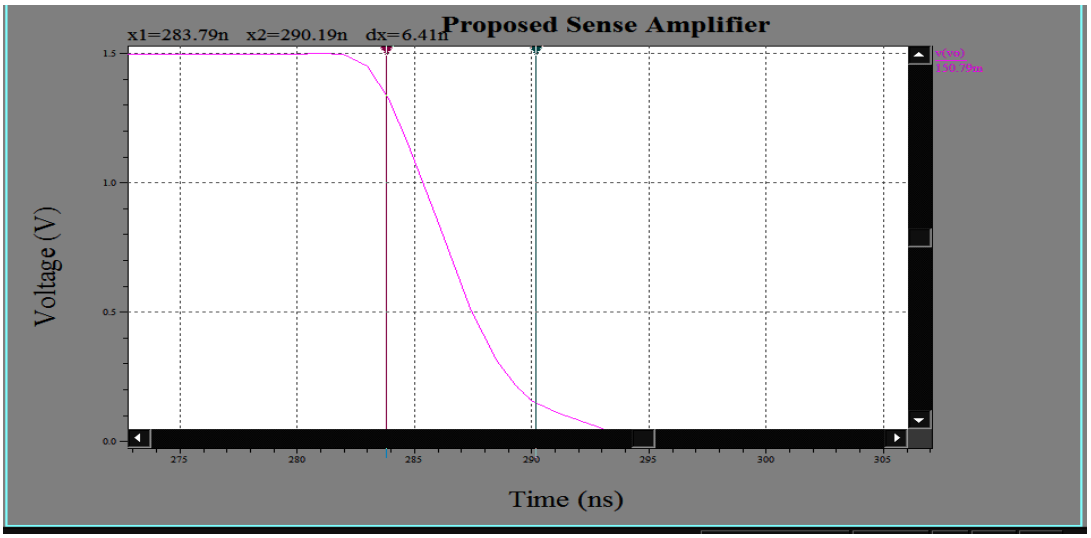

Figure5 (e) Output of Latch Sense Amplifier (Fall Times calculation)

Propagation Daley = Rise Time + Fall Time
= 13.96 +6.41
= 20.37 ns

Sense Amplifier	No of transistor	Power (nW)	Current (uA)	Propagation Delay (ns)
Proposed Sense Amplifier	9	72	23	20.37

Table 5.1 Overall Performance of Proposed Latch Sense Amplifier

VI. Conclusion

Latch type sense amplifier requires one control signal. This table shows that the proposed Current Sense Amplifier Design has less power consumption as compared to others. So this design is good design for low power applications.

For lowering the power dissipation three techniques are used that is voltage scaling, half V_{DD} precharge circuits and VTCMOS, which results in reduction of 99.8% power consumption for proposed design. Latch type sense amplifier has less power and comparable delay.

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